Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2022-08-10	yhg	1:Revision preliminary version	
V2.0	2024-7-19	yhg	1:modify the FB resistors of U6 and U7 2:modify J9502 SIM+TF pad 3:modify J8700 4G module positioning hole 4:NC R94	

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Title: Revision History

Size	Document Number	Drawn	Rev
A4	SBC3588	yhg	2

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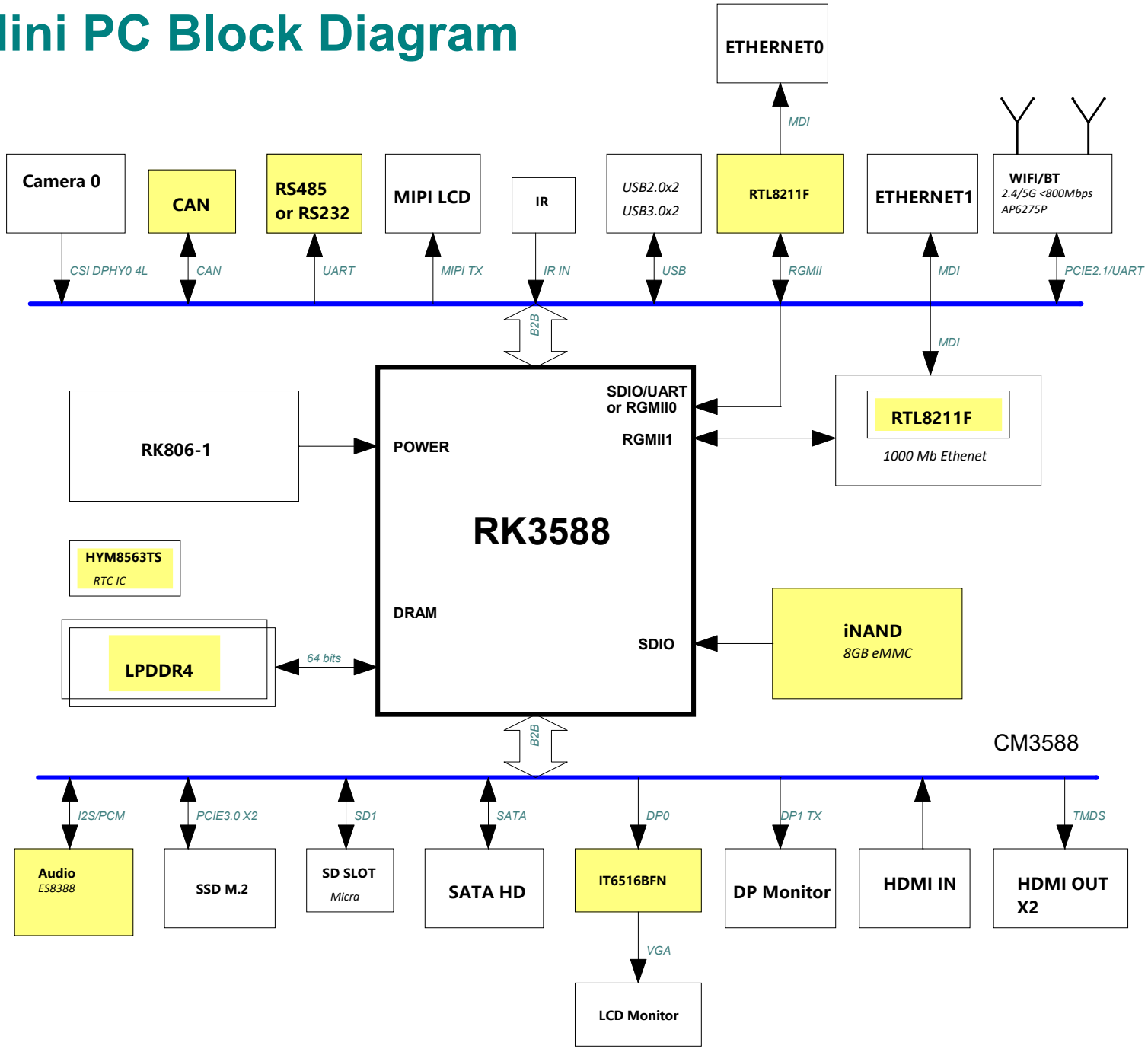
Mini PC Block Diagram



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Title: block diagram

Size: C | Document Number: SBC3588 | Drawn: yhg | Rev: 2

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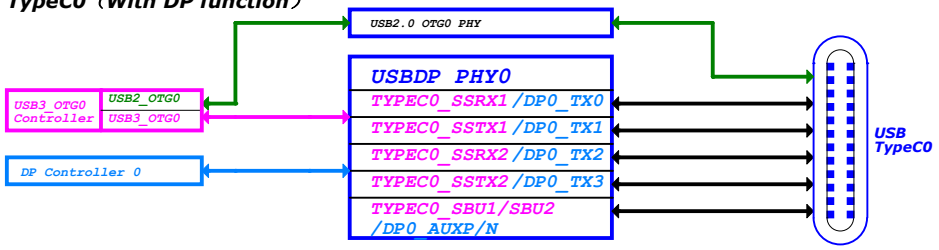
USB Controller Configure Table

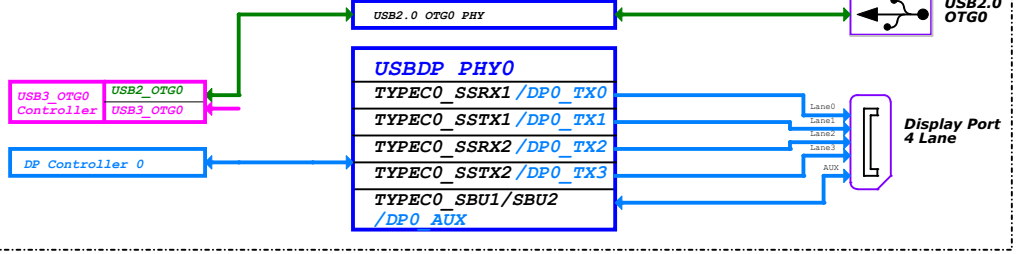
Controller Name	Pin Name	Type-C Function	DPx4Lane Function		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN		DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1N/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM			TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
USB30 OTG1 Device or Host	TYPEC1_SBU1/DP1_AUXP TYPEC1_SBU2/DP1_AUXN	TYPEC1_SBU1 TYPEC1_SBU2	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN
	TYPEC1_SSRX1P/DP1_TX0P TYPEC1_SSRX1N/DP1_TX0N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX0P DP1_TX0N		DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N
	TYPEC1_SSTX1P/DP1_TX1P TYPEC1_SSTX1N/DP1_TX1N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX1P DP1_TX1N		DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N
	TYPEC1_SSRX2P/DP1_TX2P TYPEC1_SSRX2N/DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N		DP1_TX2P DP1_TX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N
	TYPEC1_SSTX2P/DP1_TX3P TYPEC1_SSTX2N/DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N		DP1_TX3P DP1_TX3N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N
USB20 OTG1 Device or Host	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM			TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM
			OPTION1 USB30 HOST		OPTION2 USB30 HOST	OPTION3 USB30 HOST				
USB30 HOST2	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN				
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN				
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM							
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM				USB20_HOST1_DP USB20_HOST1_DM					
						TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM				

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

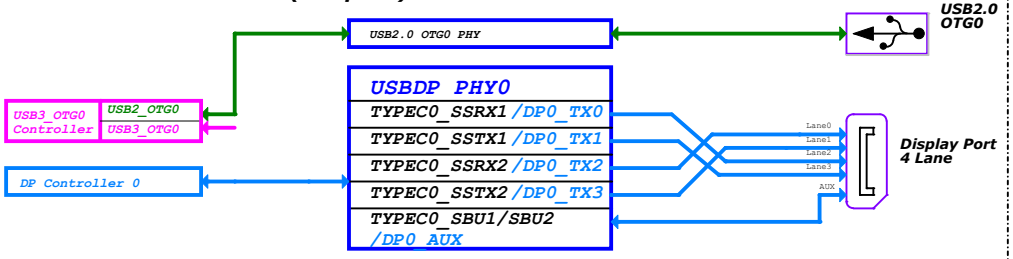
Config0:
TypeC0（With DP function）



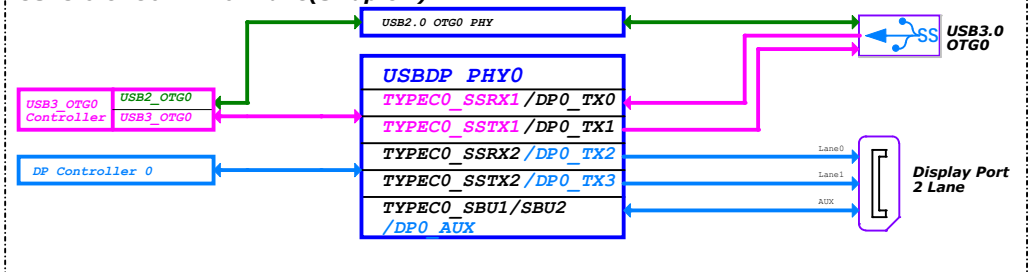
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



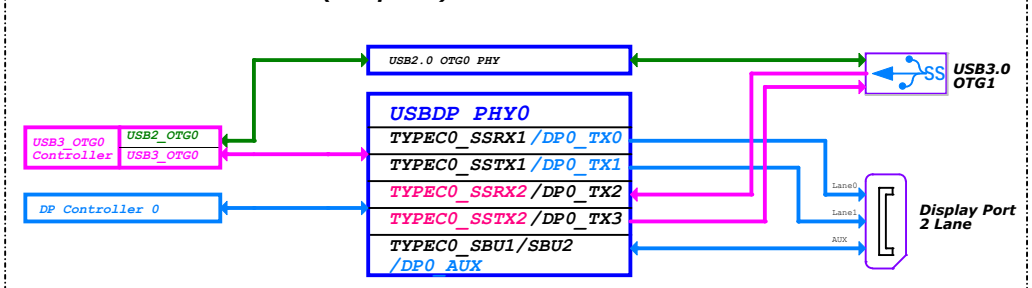
Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



Config3:
USB3.0 OTG0 + DP0 2Lane(Swap ON)



Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)



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USB/DP Configure Map
Size: A3 | Document Number: SBC3588 | Drawn: ylg | Rev: 2
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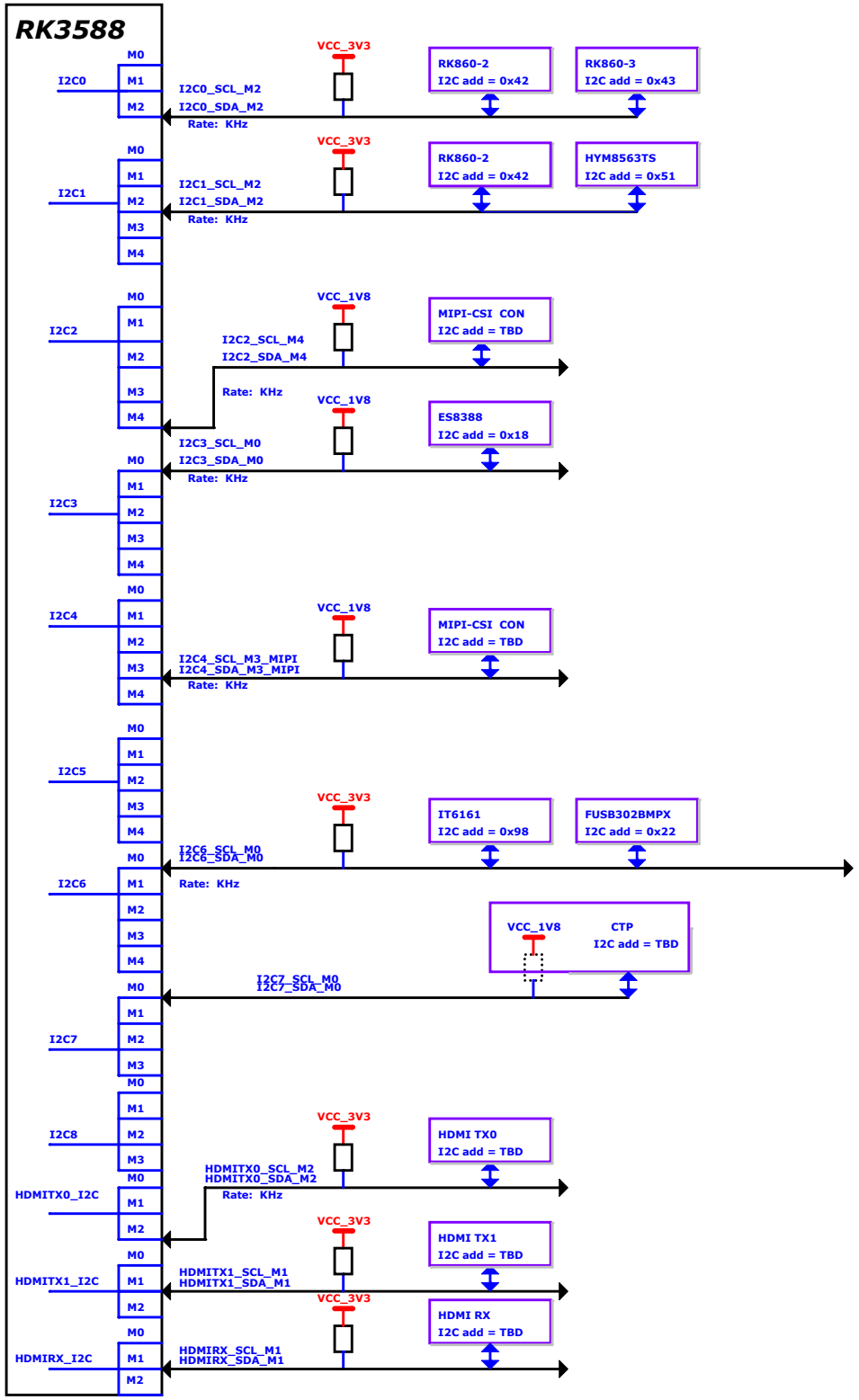
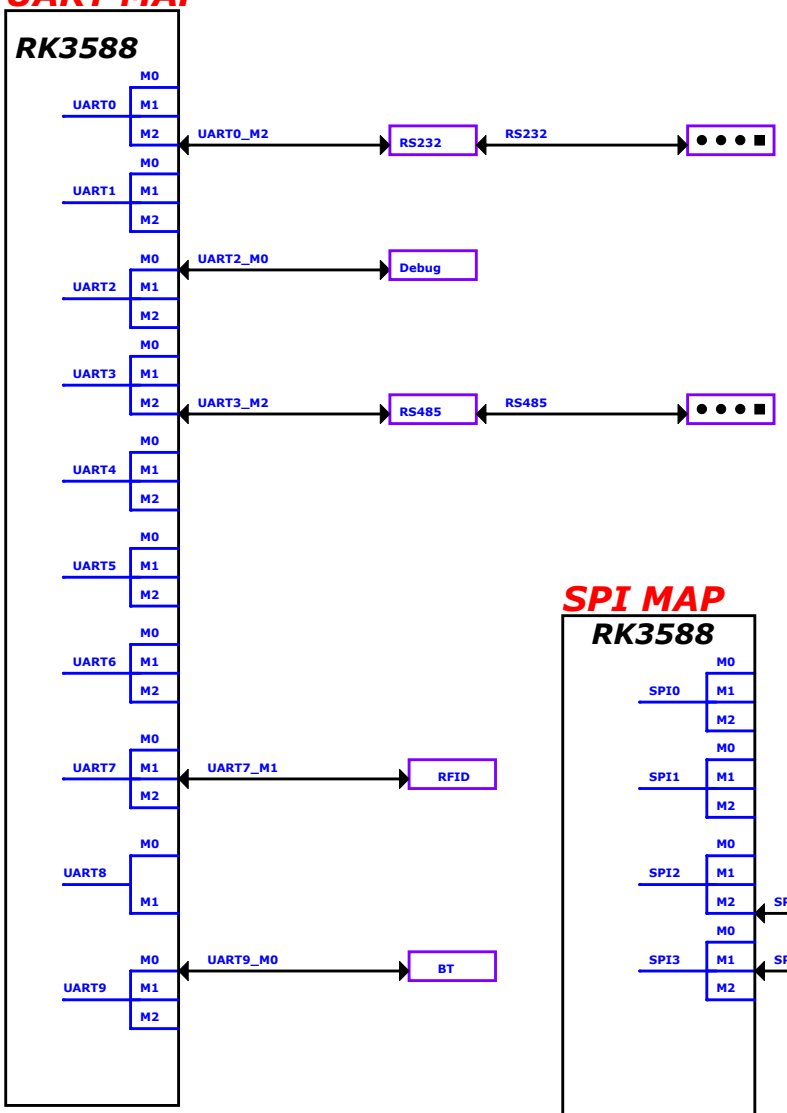
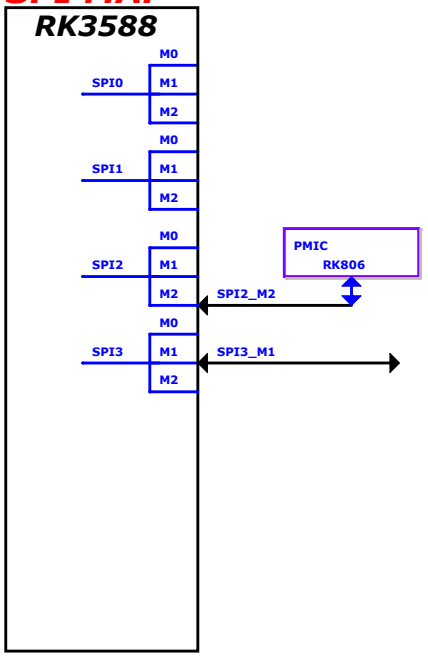
I2C MAP



UART MAP



SPI MAP



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Title: Lower-Speed Bus Map

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A2	SBC3588	yhg	2

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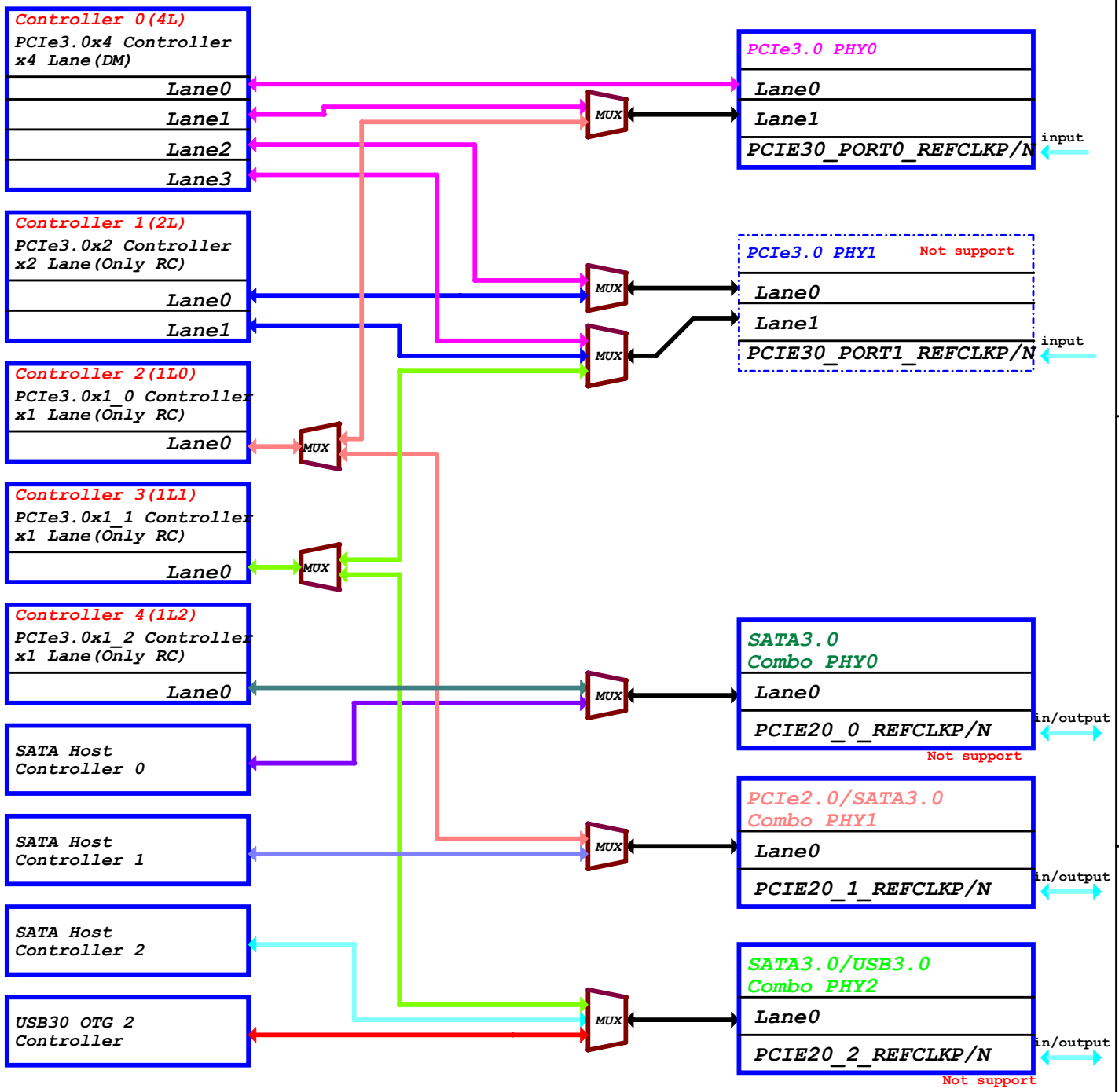
PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO & Power Pin
	OPTION	CLK LANE	DATA LANE	
PCIE30X4 RC & EP	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M* PCIE30X4_BUTTON_RSTN
	OPTION2	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	
	OPTION3	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT1_TX0 PCIE30_PORT0_RX0 PCIE30_PORT1_RX0 PCIE30_PORT0_TX1 PCIE30_PORT1_TX1 PCIE30_PORT0_RX1 PCIE30_PORT1_RX1	
PCIE30X2 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0	PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M* PCIE30X2_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIE30X1_0 RC	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M*
	OPTION2	PCIE20_1_REFCLKP PCIE20_1_REFCLKN	PCIE20_1_TXP PCIE20_1_RXP PCIE20_1_TXN PCIE20_1_RXN	PCIE30X1_0_PERSTN_M* PCIE30X1_0_BUTTON_RSTN
PCIE30X1_1 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M*
	OPTION2	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TXP PCIE20_2_RXP PCIE20_2_TXN PCIE20_2_RXN	PCIE30X1_1_PERSTN_M* PCIE30X1_1_BUTTON_RSTN
PCIE20X1_2 RC	OPTION1	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TXP PCIE20_0_RXP PCIE20_0_TXN PCIE20_0_RXN	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Note:
PCIE30_PORT*_REF_CLKP/N is input gpio

PCIE20_*_REFCLKP/N is output or input gpio

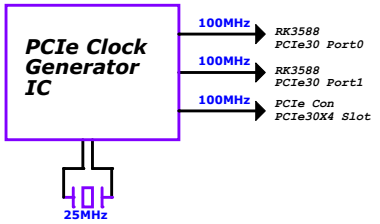
Note:
M*=Mean to M0 or M1,It's the same source,Just multiplex to M0 or M1, So,Only use one at the same time.

PCIe/SATA Function Combination

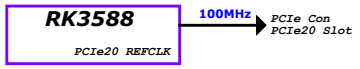
Function Combination

Function Item	PCIEX4	PCIEX2	PCIEX1	SATA
Option1	1(DM)	0	3(RC)	0
Option2	1(DM)	0	2(RC)	1
Option3	1(DM)	0	1(RC)	2
Option4	1(DM)	0	0	3
Option5	0	1(DM)+1(RC)	3(RC)	0
Option6	0	1(DM)+1(RC)	2(RC)	1
Option7	0	1(DM)+1(RC)	1(RC)	2
Option8	0	1(DM)+1(RC)	0	3
Option9	0	1(DM)	4(RC)	1
Option10	0	1(DM)	3(RC)	2
Option11	0	1(DM)	2(RC)	3
Option12	0	0	1(DM)+4(RC)	2
Option13	0	0	1(DM)+3(RC)	3

PCIe3.0 REFCLK



PCIe2.0 REFCLK



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Title: PCIE Fun Map			
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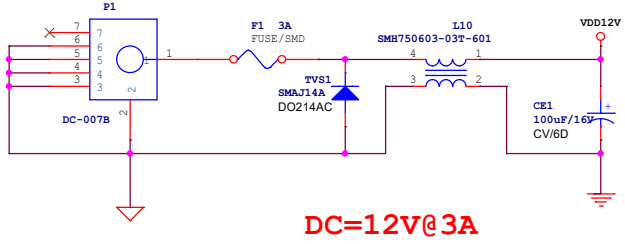
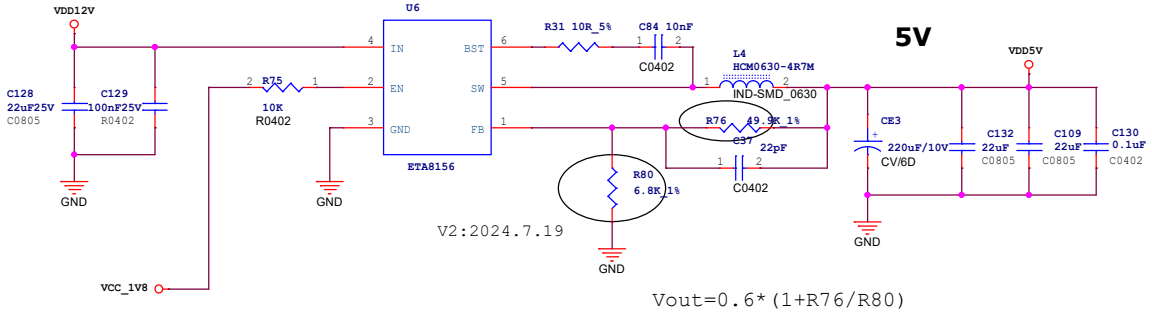
Main Power



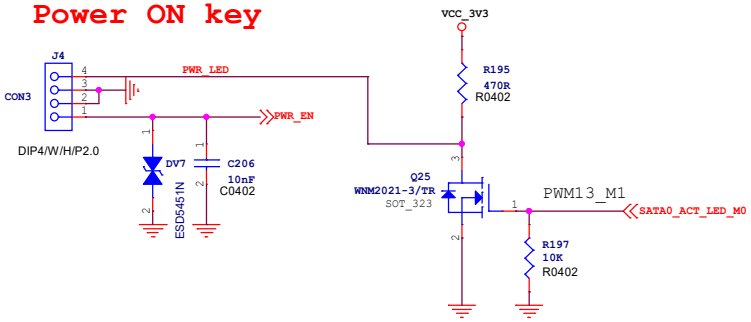
DC=12V@3A

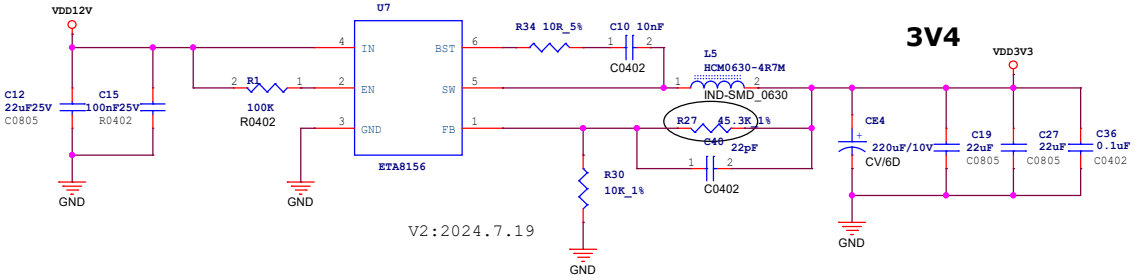


V2:2024.7.19

Vout=0.6*(1+R76/R80)

Power ON key

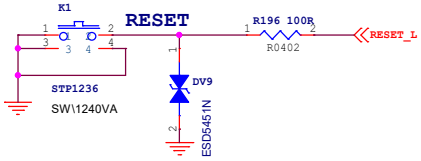


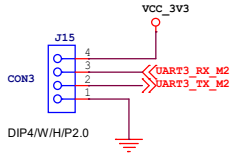


V2:2024.7.19

Vout=0.6*(1+R27/R30)

KEY





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Title: Power/KEY/IR			
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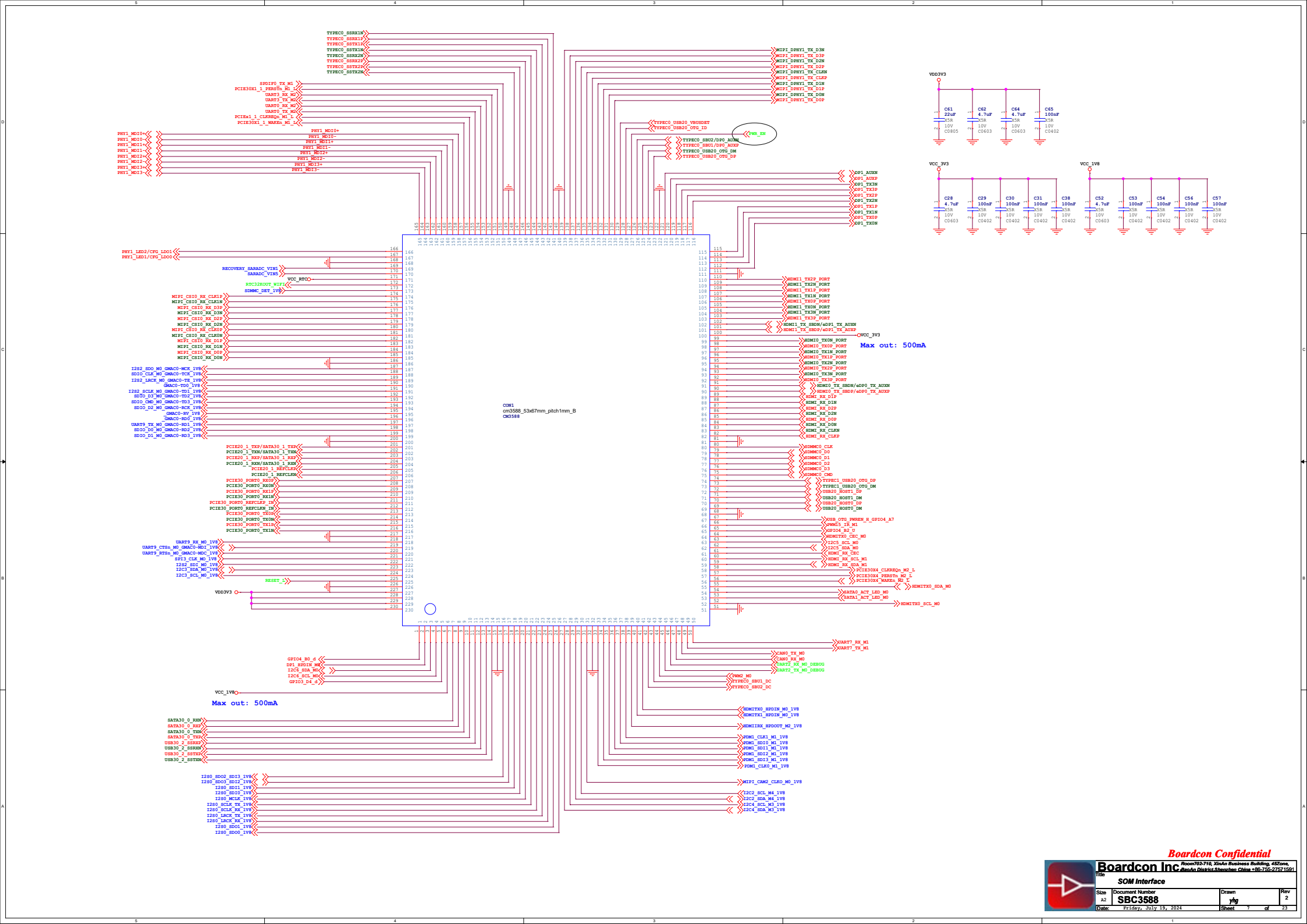

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Title: SOM Interface			
Size: A2	Document Number: SBC3588	Drawn: yhg	Rev: 2
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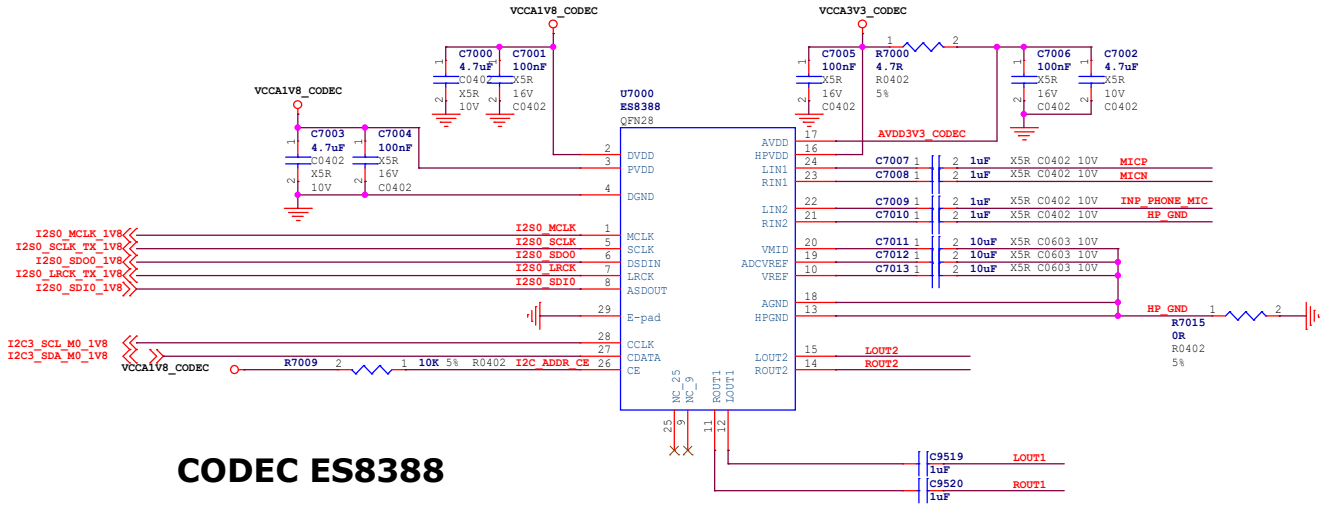
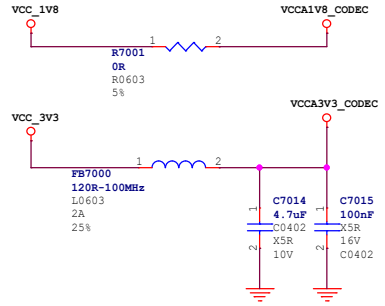
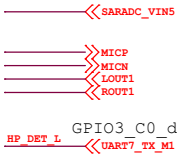
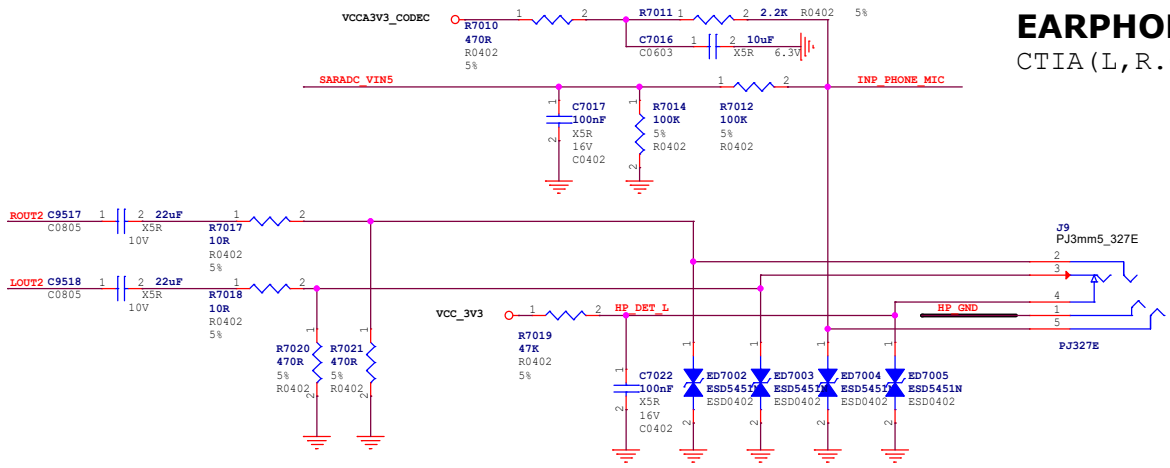


CODEC ES8388







EARPHONE

CTIA(L,R.G,M)

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Title: Audio Codec/SPDIFO

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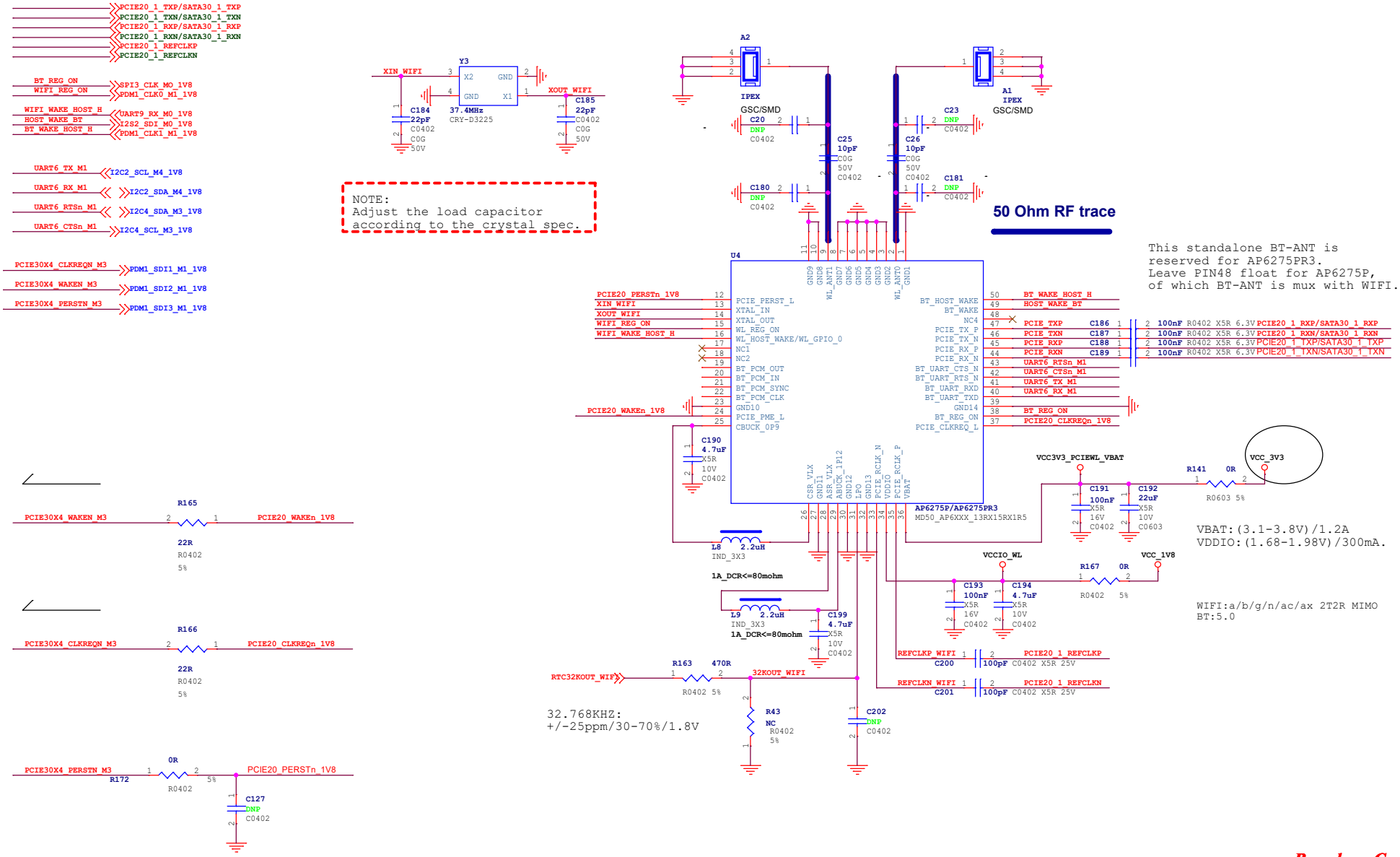
PCIe WIFI6/BT Module-2T2R



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Title	WIFI/BT-PCIE_2T2R		
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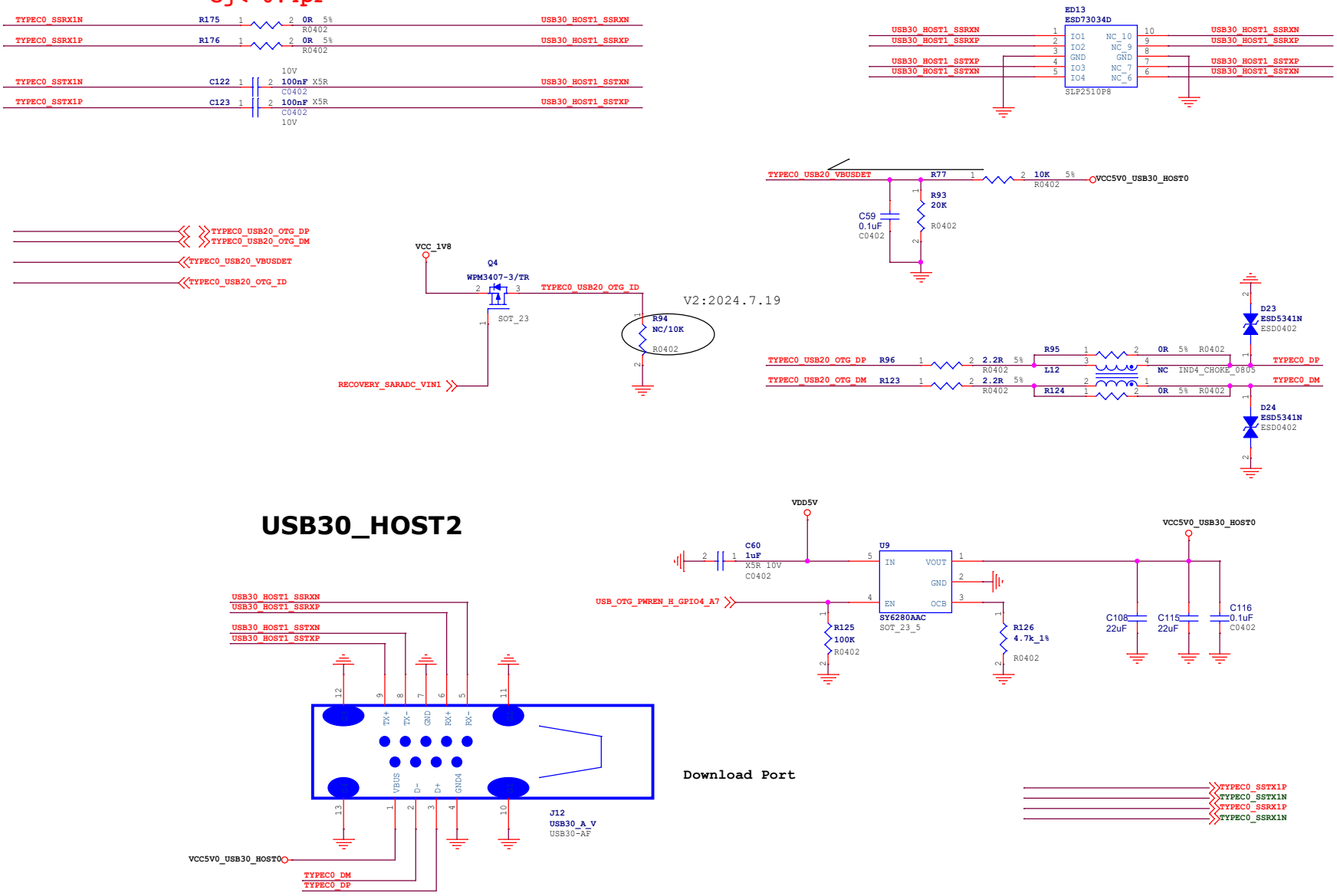
Cj<=0.4pF

Note:
USB3.0信号的ESD不能随便换掉
如需换那么必须选择相同的规格。



USB30_HOST2

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Title	Rear USB3.0 with download		
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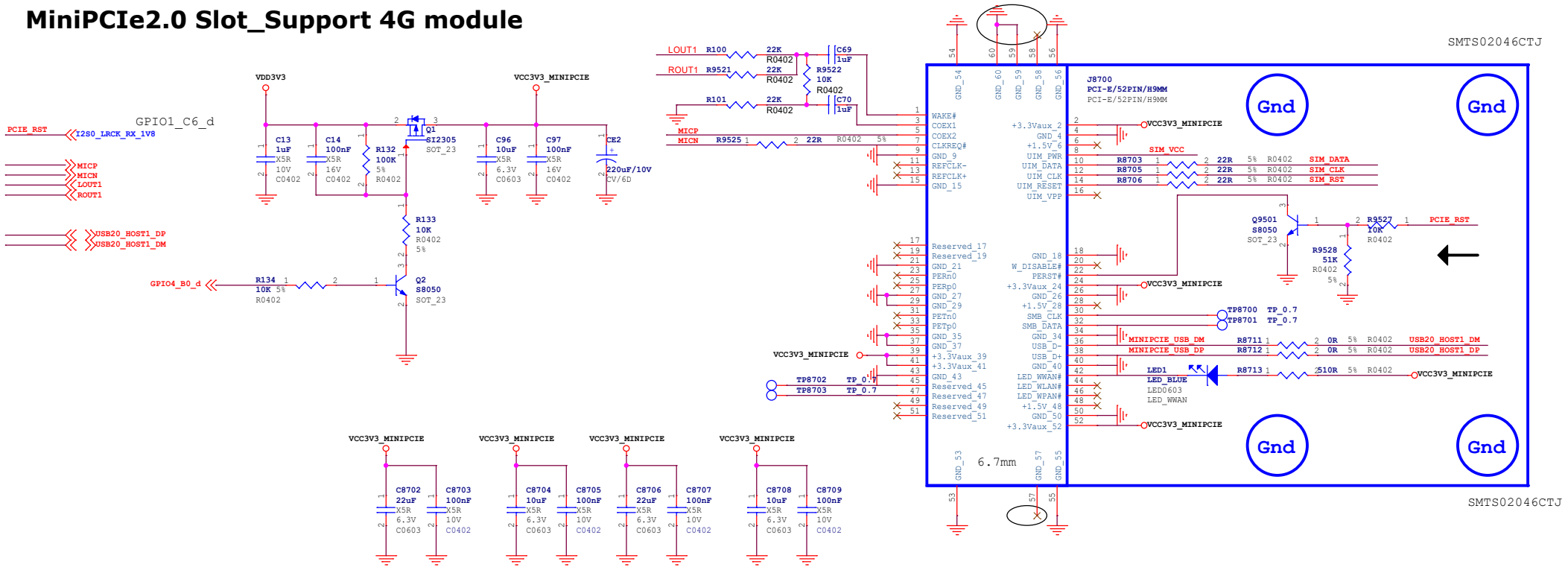
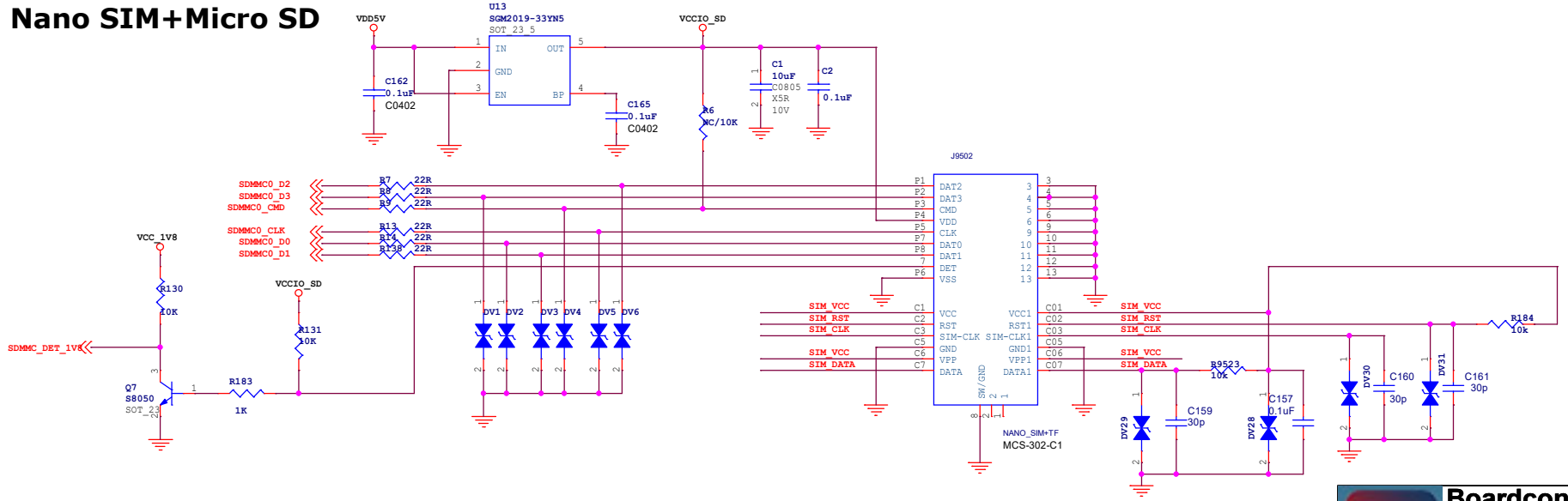
MiniPCIe2.0 Slot_Support 4G module



Nano SIM+Micro SD



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Title: MiniPCIe Slot/Micra SD			
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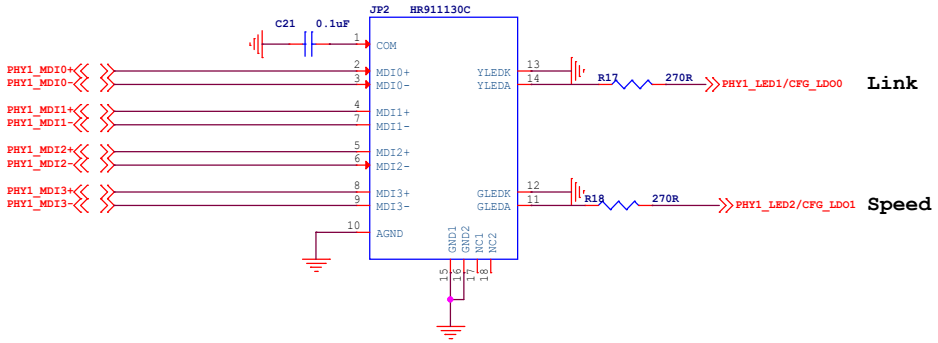
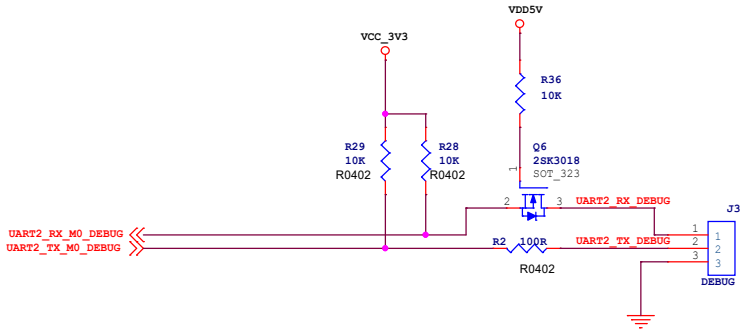
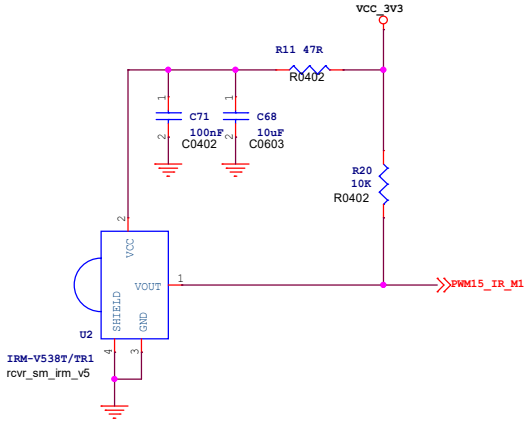
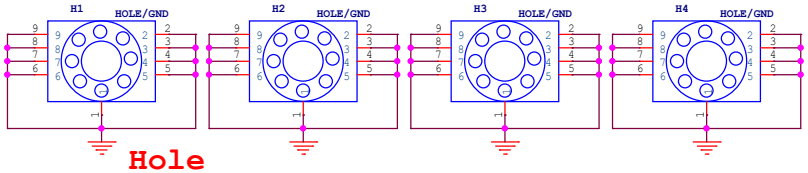
Ethernet1

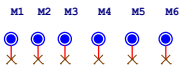






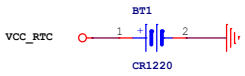


Hole



Mark

RTC Power



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Title: UART/RS485/CAN/Ethernet			
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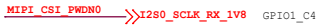
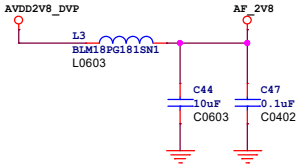
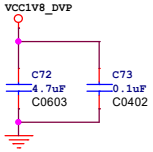
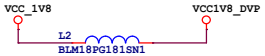
MIPI Camera

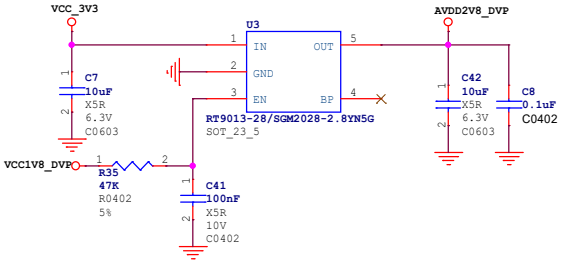


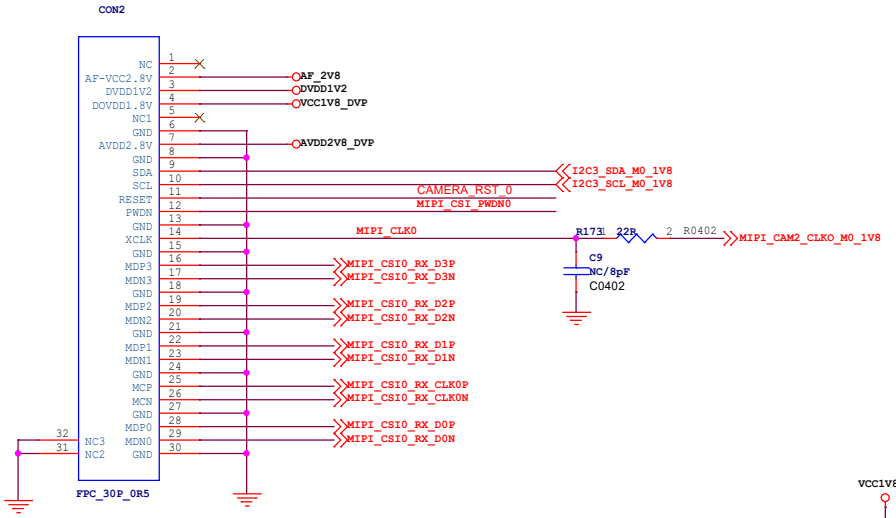


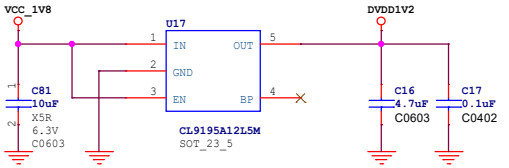


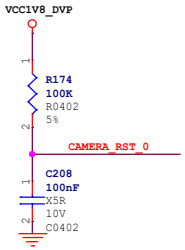
MIPI-CSI_DPHY0_RX Interface











Camera 0

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Title	VI-MIPI Camera		
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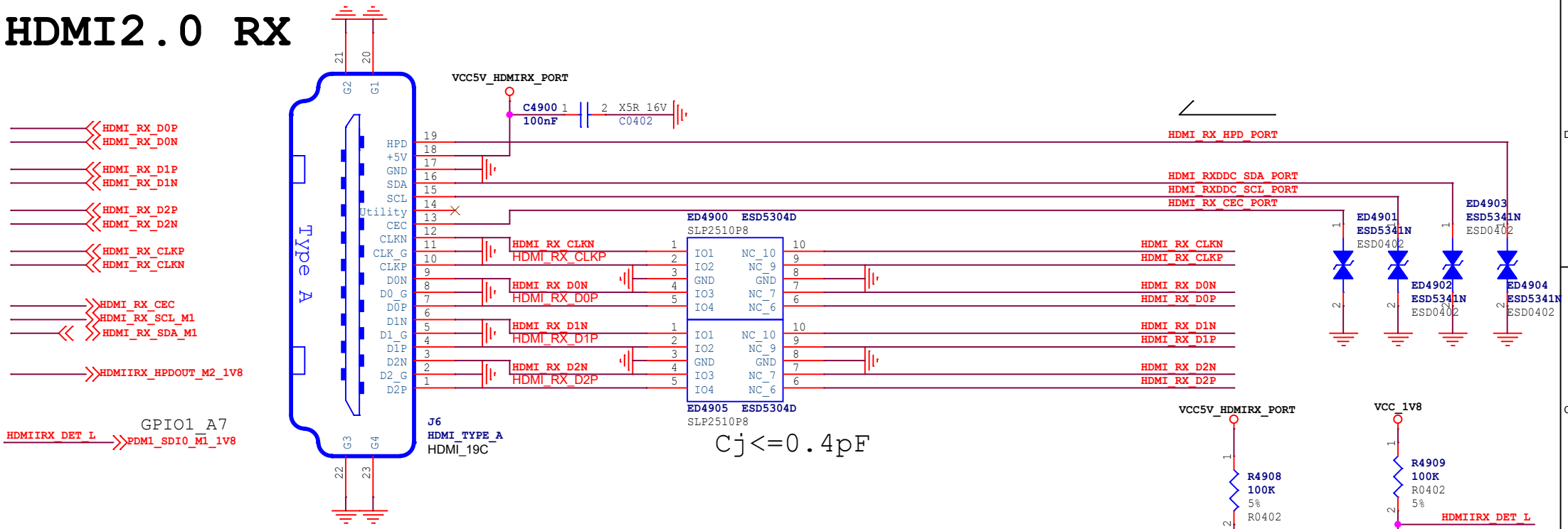
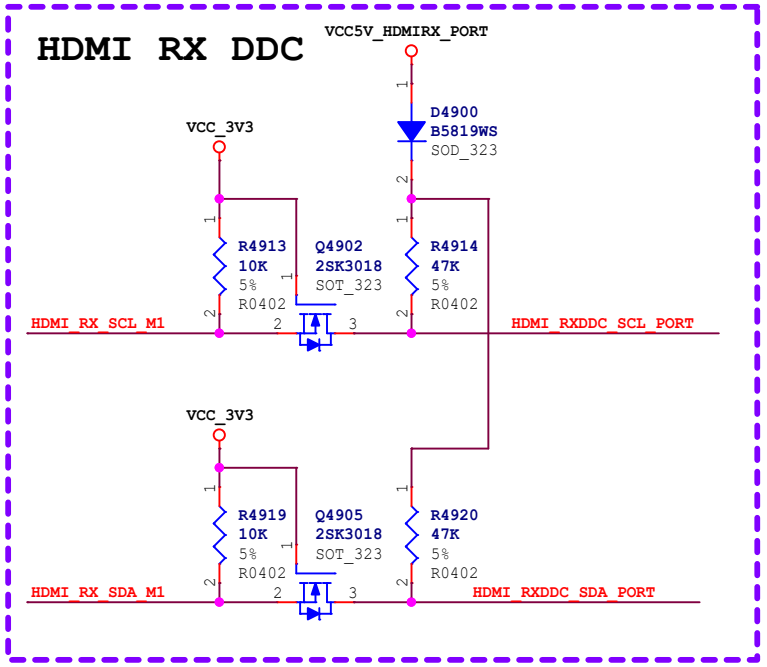
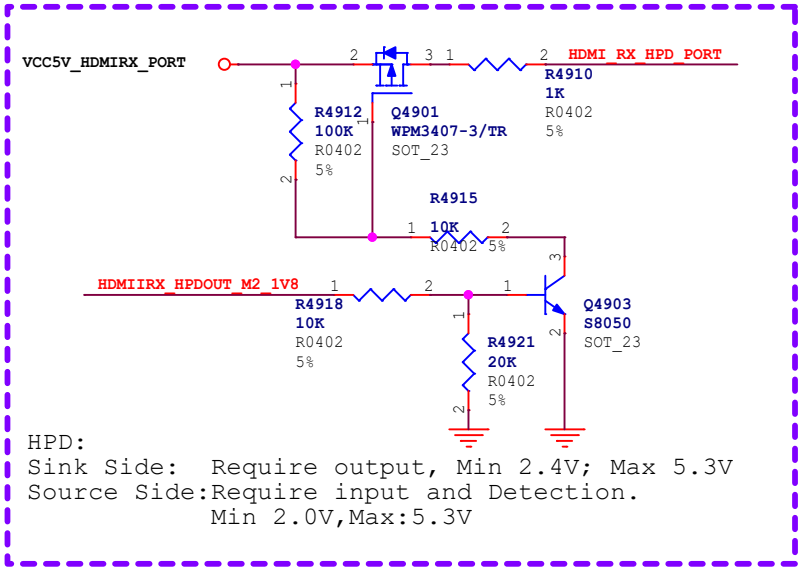
HDMI2.0 RX

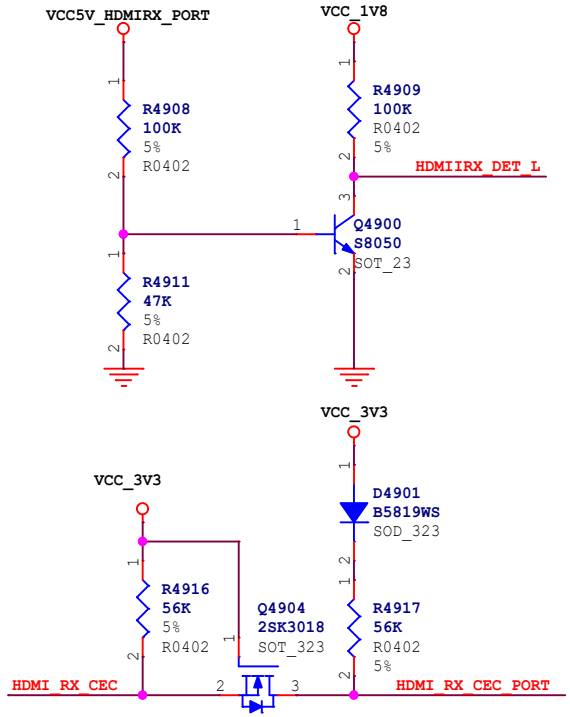


HDMI RX DDC





HPD:
Sink Side: Require output, Min 2.4V; Max 5.3V
Source Side:Require input and Detection.
Min 2.0V,Max:5.3V



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Title: VI-HDMI2.0 RX			
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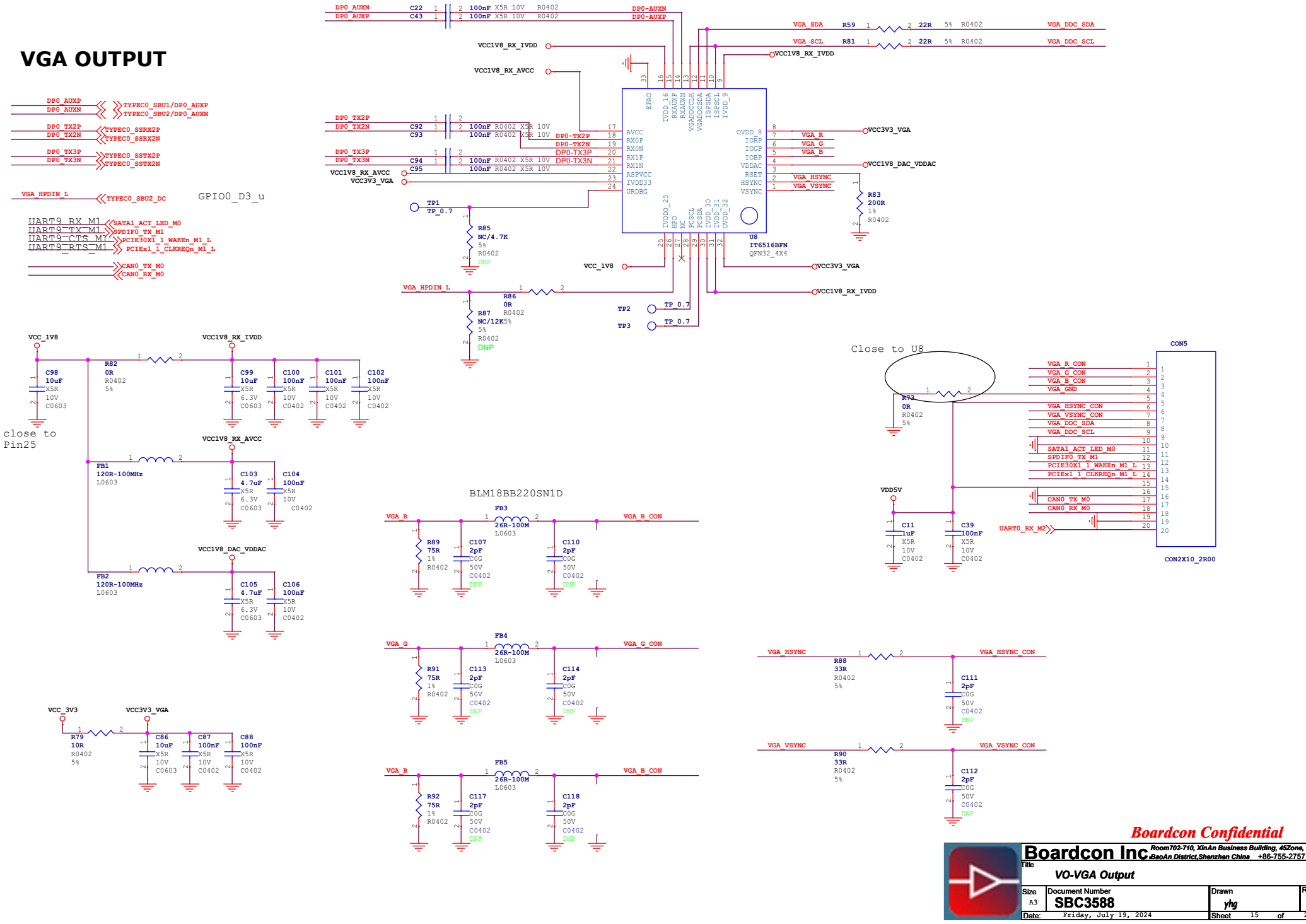
VGA OUTPUT



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Title: VO-VGA Output			
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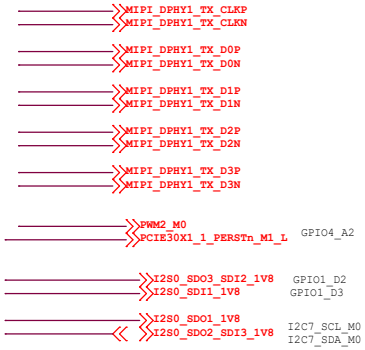

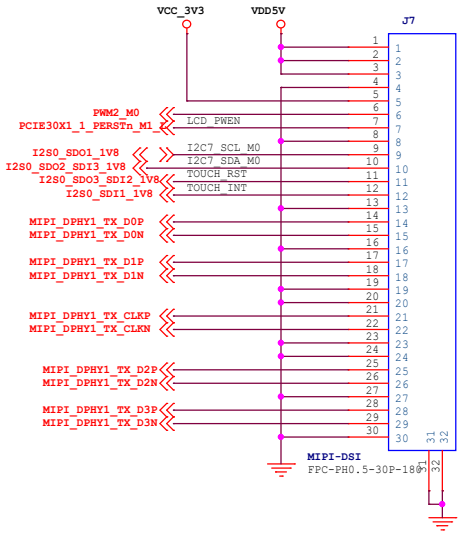

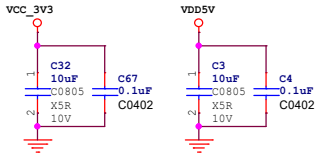

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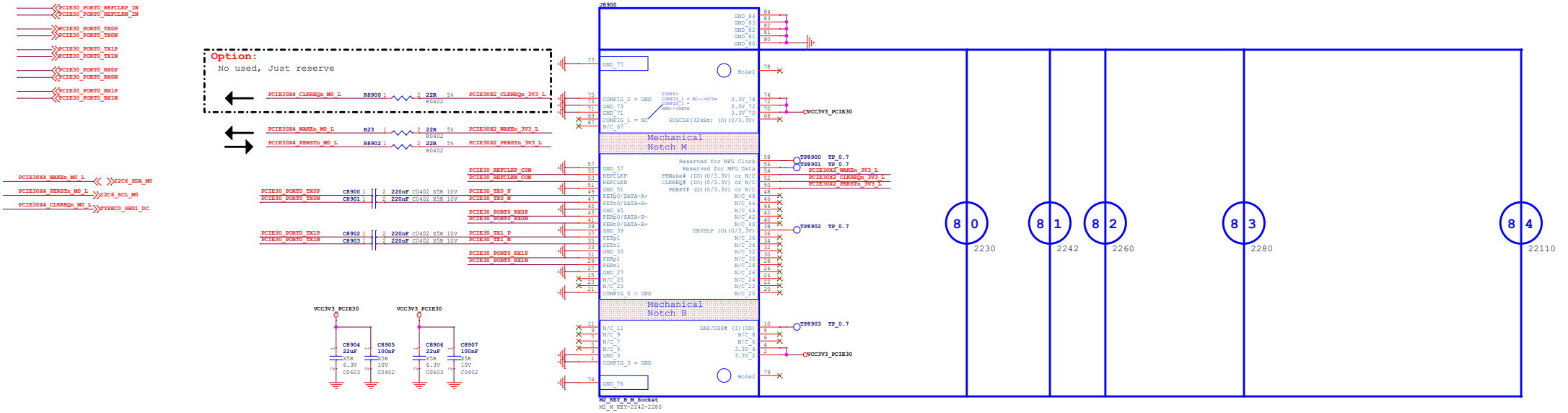
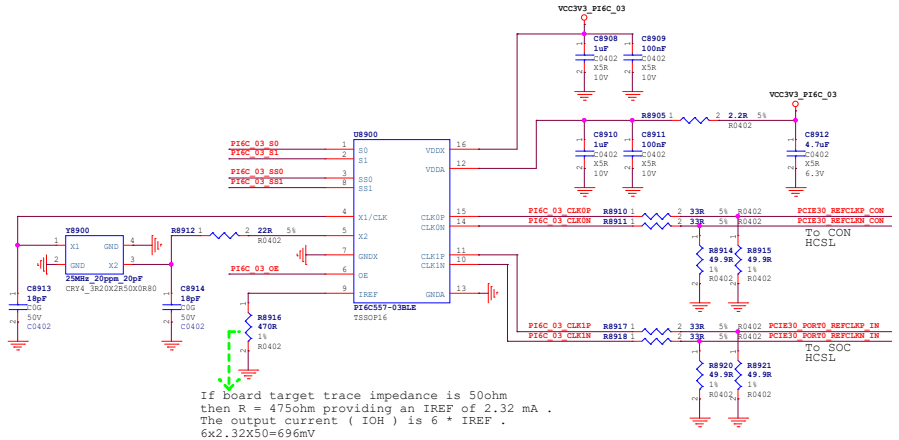
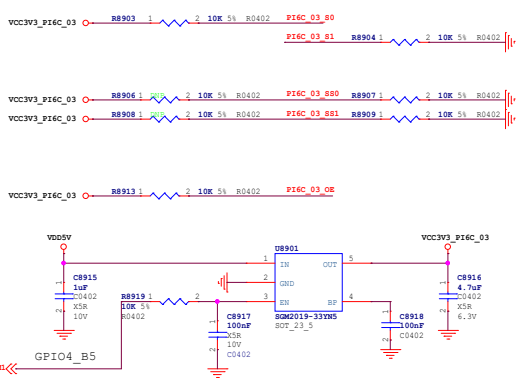
M.2_PCIe3.0 x 2Lanes



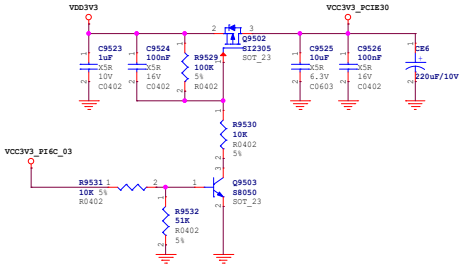
Crystal Generator





PI6C_S1	PI6C_S0	Out Freq
0	1	100MHz

PI6C_SS1	PI6C_SS0	Spread %
0	0	No Spread
0	1	-0.5
1	0	-1.0
1	1	No Spread



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Title: PCIE-M.2/SATA			
Size: A2	Document Number: SBC3588	Drawn: yhg	Rev: 2
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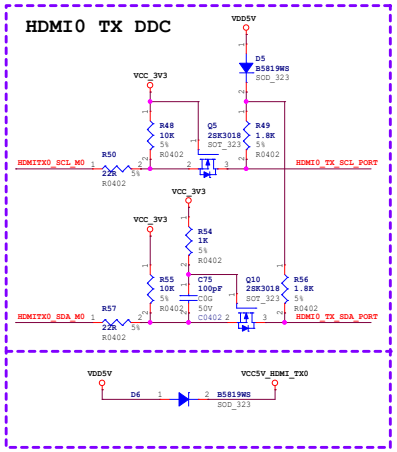
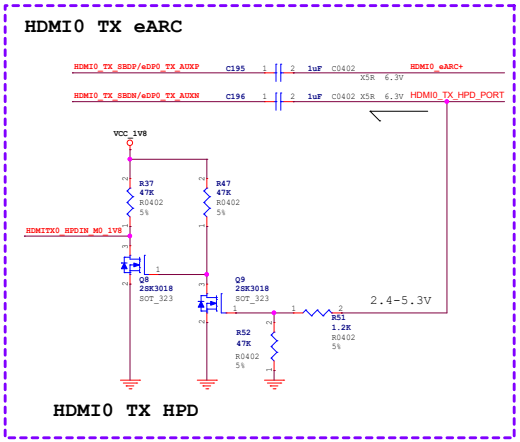
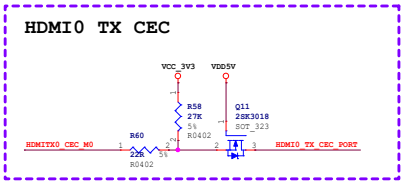
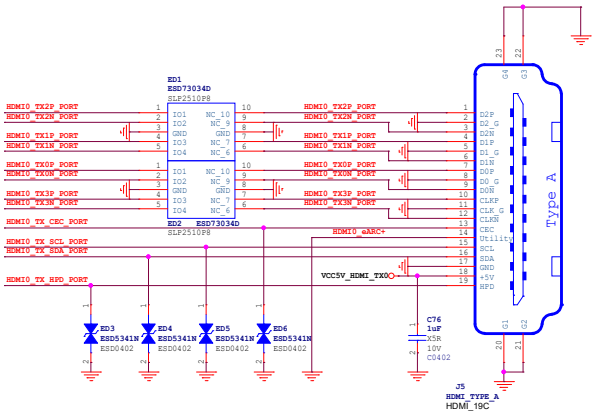
HDMI TX0

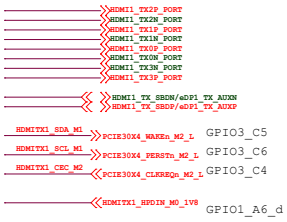


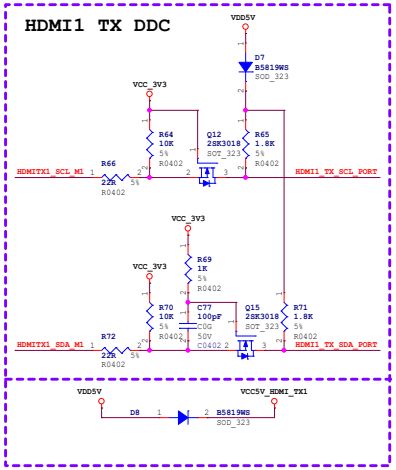


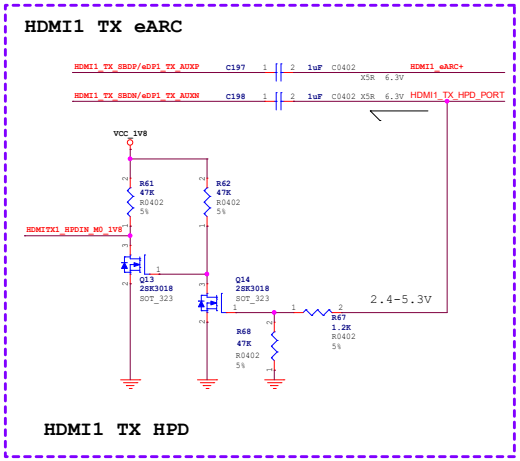


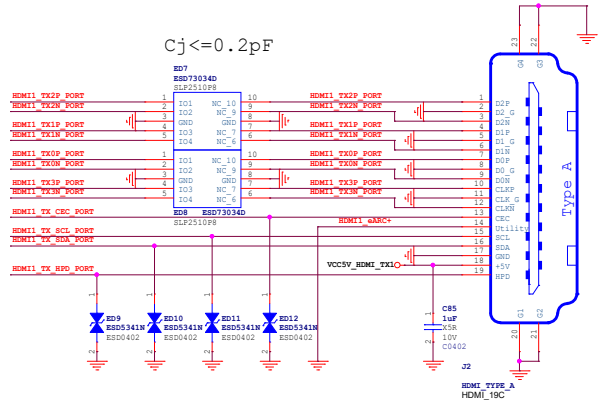


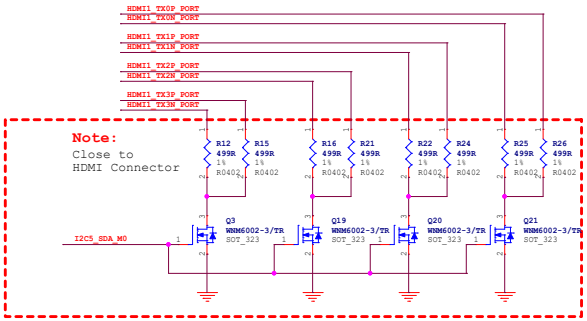
HDMI TX1

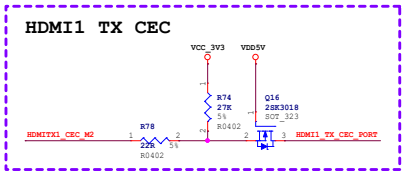












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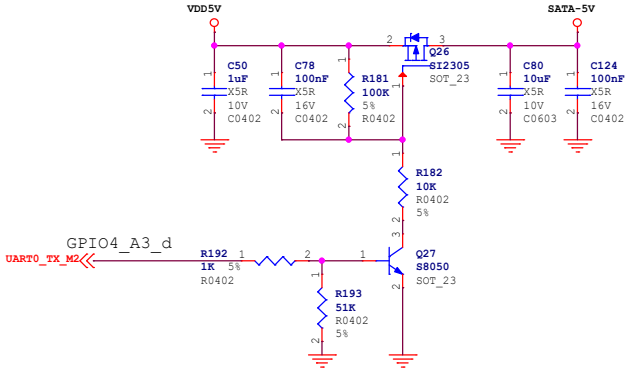
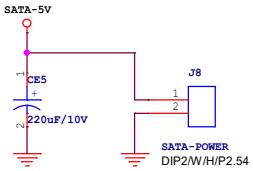
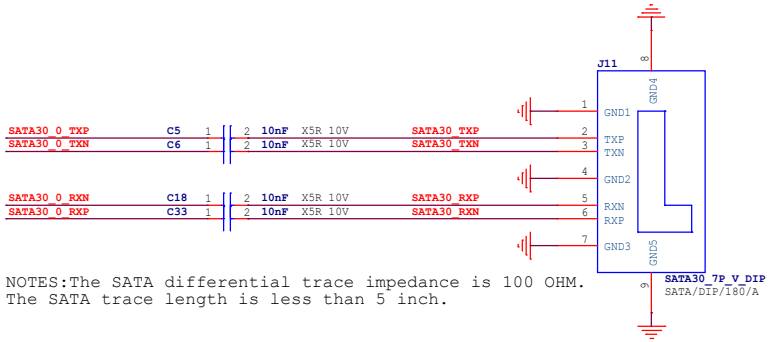
SATA



SATA POWER





NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

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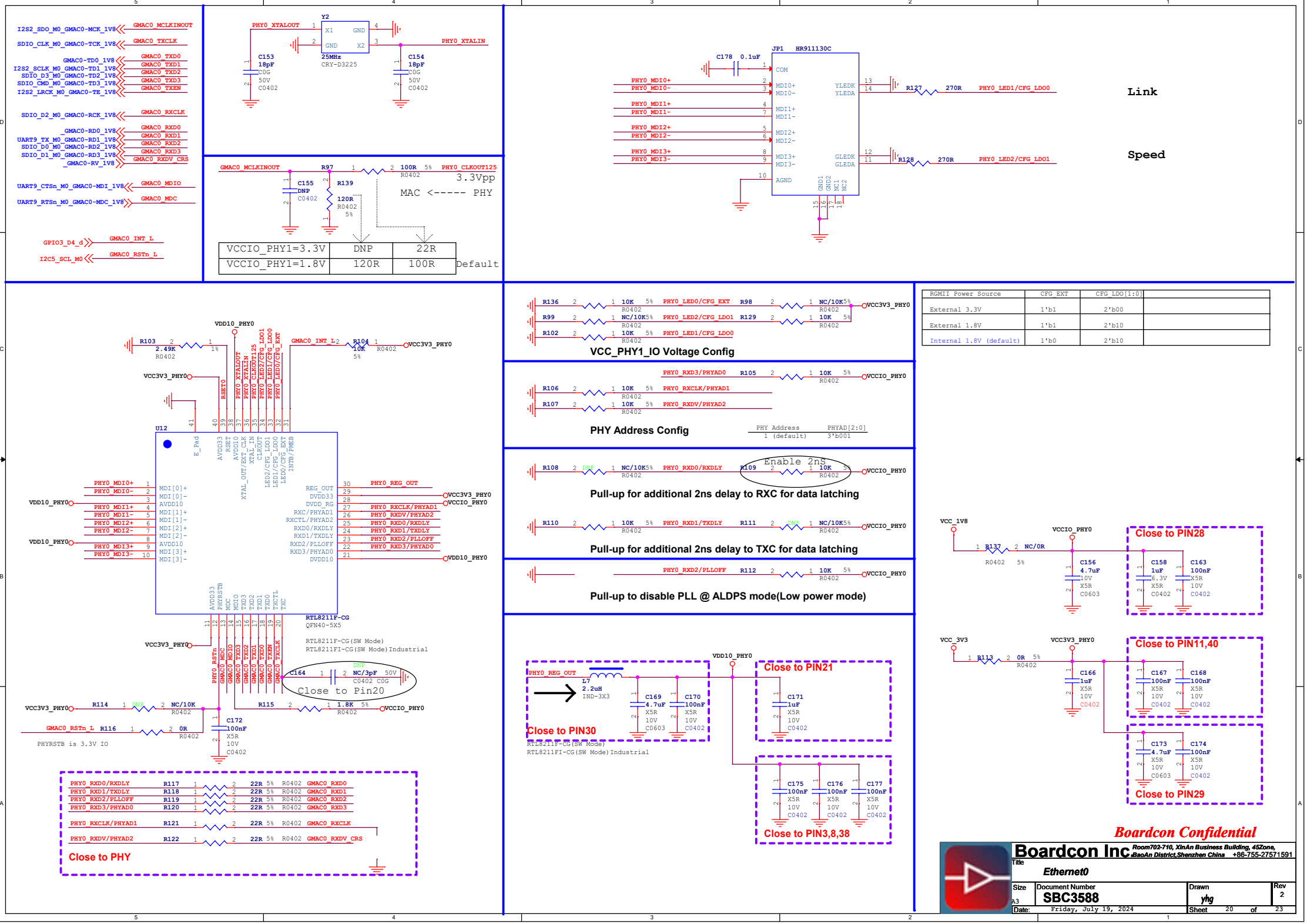
I2S2_SDO_M0_GMAC0-MCK_1V8
GMAC0_MCLKINOUT
SDIO_CLK_M0_GMAC0-TCK_1V8
GMAC0_TXCLK
GMAC0-TD0_1V8
GMAC0_TXD0
I2S2_SCLK_M0_GMAC0-TD1_1V8
GMAC0_TXD1
SDIO_D3_M0_GMAC0-TD2_1V8
GMAC0_TXD2
SDIO_CMD_M0_GMAC0-TD3_1V8
GMAC0_TXD3
I2S2_LRCK_M0_GMAC0-TE_1V8
GMAC0_TXEN
SDIO_D2_M0_GMAC0-RCK_1V8
GMAC0_RXCLK
GMAC0-RD0_1V8
GMAC0_RXD0
UART9_TX_M0_GMAC0-RD1_1V8
GMAC0_RXD1
SDIO_D0_M0_GMAC0-RD2_1V8
GMAC0_RXD2
SDIO_D1_M0_GMAC0-RD3_1V8
GMAC0_RXD3
GMAC0-RV_1V8
GMAC0_RXDV_CRS
UART9_CTSn_M0_GMAC0-MDI_1V8
GMAC0_MDIO
UART9_RTSn_M0_GMAC0-MDC_1V8
GMAC0_MDC
GPIO3_D4_d
GMAC0_INT_L
I2C5_SCL_M0
GMAC0_RSTn_L
Y2
PHY0_XTALOUT
PHY0_XTALIN
X1
X2
GND
25MHz
CRY-D3225
C153
18pF
C0G
50V
C0402
C154
18pF
C0G
50V
C0402
GMAC0_MCLKINOUT
R97
100R
5%
R0402
PHY0_CLKOUT125
3.3Vpp
MAC <----- PHY
C155
DNP
C0402
R139
120R
R0402
5%
VCCIO_PHY1=3.3V
DNP
22R
VCCIO_PHY1=1.8V
120R
100R
Default
JP1
HR911130C
C178
0.1uF
COM
PHY0_MDI0+
PHY0_MDI0-
MDI0+
MDI0-
YLEDK
YLEDA
R127
270R
PHY0_LED1/CFG_LDO0
Link
PHY0_MDI1+
PHY0_MDI1-
MDI1+
MDI1-
PHY0_MDI2+
PHY0_MDI2-
MDI2+
MDI2-
PHY0_MDI3+
PHY0_MDI3-
MDI3+
MDI3-
GLEDK
GLEDA
R128
270R
PHY0_LED2/CFG_LDO1
Speed
AGND
GND1
GND2
NC1
NC2
VDD10_PHY0
R103
2.49K
1%
R0402
VCC3V3_PHY0
RSET0
PHY0_XTALOUT
PHY0_XTALIN
PHY0_CLKOUT125
PHY0_LED2/CFG_LDO1
PHY0_LED1/CFG_LDO0
PHY0_LED0/CFG_EXT
GMAC0_INT_L
R104
10K
5%
R0402
U12
E_Pad
AVDD33
RSET
AVDD10
XTAL_OUT/EXT_CLK
XTAL_IN
CLKOUT
LED2/CFG_LDO1
LED1/CFG_LDO0
LED0/CFG_EXT
INTB/PMEB
MDI[0]+
MDI[0]-
AVDD10
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
AVDD10
MDI[3]+
MDI[3]-
REG_OUT
DVDD33
DVDD_RG
RXC/PHYAD1
RXCTL/PHYAD2
RXD0/RXDLY
RXD1/TXDLY
RXD2/PLLOFF
RXD3/PHYAD0
DVDD10
PHY0_REG_OUT
PHY0_RXCLK/PHYAD1
PHY0_RXDV/PHYAD2
PHY0_RXD0/RXDLY
PHY0_RXD1/TXDLY
PHY0_RXD2/PLLOFF
PHY0_RXD3/PHYAD0
AVDD33
PHYRSTB
MDC
MDIO
TXD3
TXD2
TXD1
TXD0
TXCTL
TXC
RTL8211F-CG
QFN40-5X5
RTL8211F-CG(SW Mode)
RTL8211FI-CG(SW Mode)Industrial
C164
DNP
NC/3pF
50V
C0402 C0G
Close to Pin20
R114
DNP
NC/10K
R0402
R115
1.8K
5%
R0402
VCCIO_PHY0
C172
100nF
X5R
10V
C0402
GMAC0_RSTn_L
R116
0R
R0402
PHYRSTB is 3.3V IO
PHY0_RXD0/RXDLY
R117
22R
5%
R0402
GMAC0_RXD0
PHY0_RXD1/TXDLY
R118
GMAC0_RXD1
PHY0_RXD2/PLLOFF
R119
GMAC0_RXD2
PHY0_RXD3/PHYAD0
R120
GMAC0_RXD3
PHY0_RXCLK/PHYAD1
R121
GMAC0_RXCLK
PHY0_RXDV/PHYAD2
R122
GMAC0_RXDV_CRS
Close to PHY
R136
10K
R0402
PHY0_LED0/CFG_EXT
R98
NC/10K
R99
PHY0_LED2/CFG_LDO1
R129
R102
PHY0_LED1/CFG_LDO0
VCC_PHY1_IO Voltage Config
PHY0_RXD3/PHYAD0
R105
VCCIO_PHY0
R106
PHY0_RXCLK/PHYAD1
R107
PHY0_RXDV/PHYAD2
PHY Address Config
PHY Address
PHYAD[2:0]
1 (default)
3'b001
R108
PHY0_RXD0/RXDLY
R109
Enable 2ns
Pull-up for additional 2ns delay to RXC for data latching
R110
PHY0_RXD1/TXDLY
R111
Pull-up for additional 2ns delay to TXC for data latching
PHY0_RXD2/PLLOFF
R112
Pull-up to disable PLL @ ALDPS mode(Low power mode)
PHY0_REG_OUT
L7
2.2uH
IND-3X3
C169
4.7uF
C0603
C170
100nF
C171
1uF
Close to PIN21
Close to PIN30
C175
C176
C177
Close to PIN3,8,38
RGMII Power Source
CFG_EXT
CFG_LDO[1:0]
External 3.3V
1'b1
2'b00
External 1.8V
2'b10
Internal 1.8V (default)
1'b0
VCC_1V8
R137
NC/0R
C156
4.7uF
C158
1uF
6.3V
C163
Close to PIN28
VCC_3V3
R113
0R
C166
1uF
C167
100nF
C168
Close to PIN11,40
C173
4.7uF
C174
Close to PIN29
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Title
Ethernet0
Size
A3
Document Number
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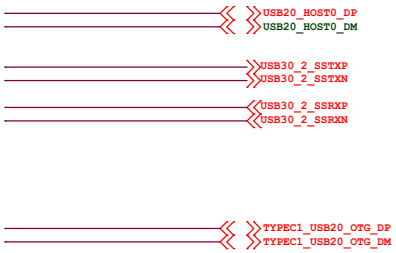
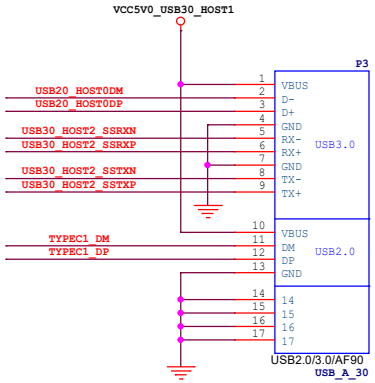
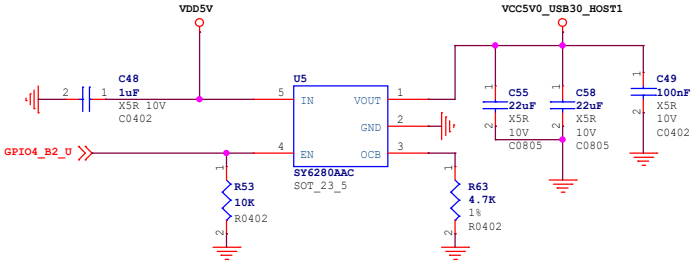
USB30+USB2.0

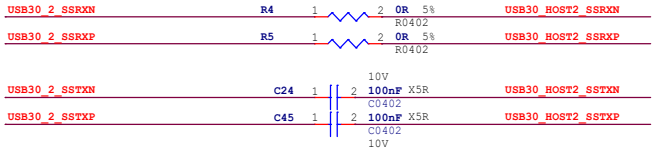


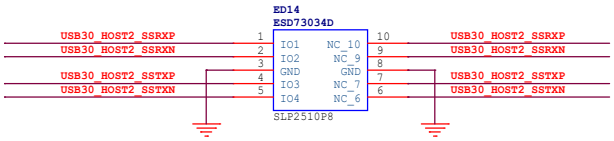


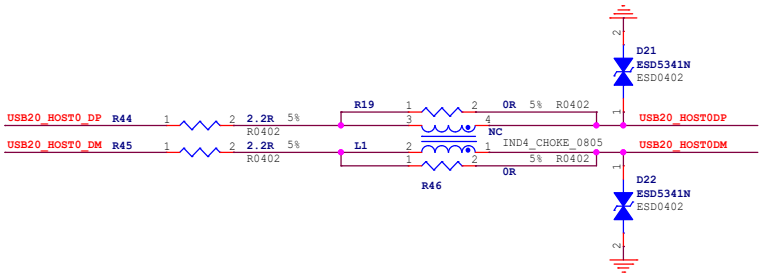


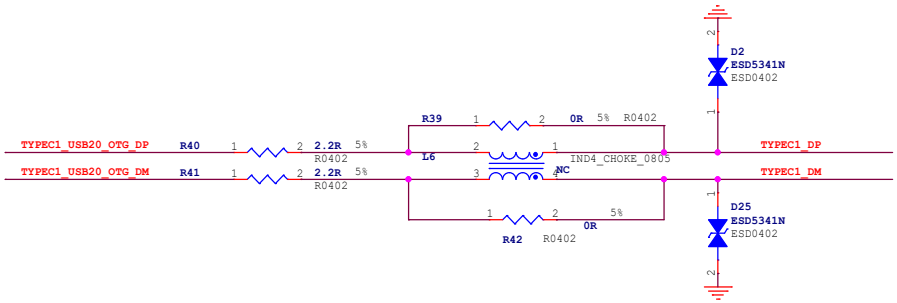
Note:
USB3.0信号的ESD不能随便换掉
如需换那么必须选择相同的规格。

Cj<=0.4pF









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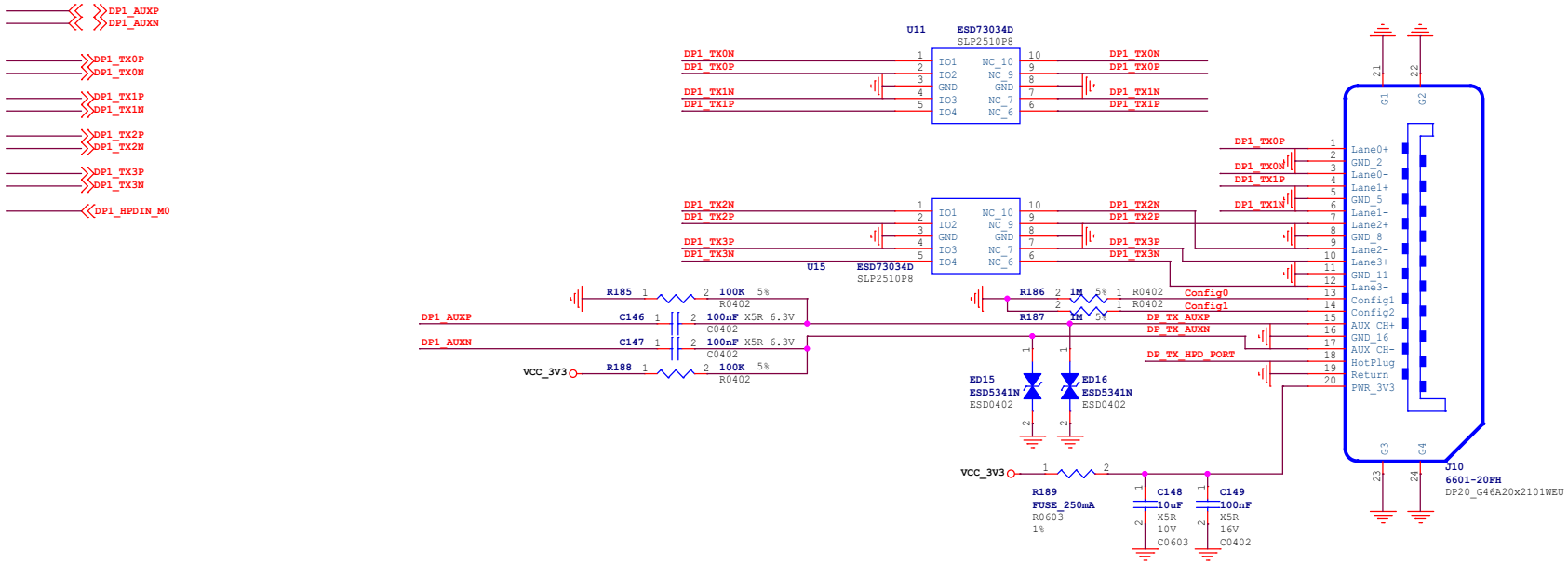
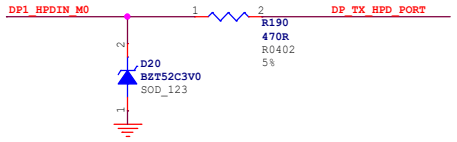
DisplayPort TX



DP_TX_HPD

HPD Voltage:2.25-3.6V



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